



## **IBM Announces a New Platform for Chip Design Verification**

### ***RuleBase PE Finds More "Evasive Bugs" Throughout the Design Cycle***

Paris, France, February 17, 2004 -- IBM announced today a new verification platform that will allow engineers to harness the power of parallel computing, thereby enabling them to rapidly verify complex chip designs and ensure their new devices work the way they should.

RuleBase Parallel Edition (PE) is a breakthrough static assertion-based verification solution, where a design is validated against its functional specification, as captured by user-specified "assertions". It is based on parallel formal and semi-formal verification algorithms that were developed in IBM Research labs at Haifa, Israel and is available to customers and partners through IBM Engineering & Technology Services.

"RuleBase PE, built on IBM's new parallel formal verification technology, is an industrial-strength tool that gives designers and verification engineers an upper hand when it comes to finding evasive design bugs throughout the design cycle," said Dr. Yaron Wolfsthal, manager of the IBM Formal Methods group at the IBM Haifa Labs, where RuleBase Parallel Edition was conceived. "We can verify large-scale designs at a fraction of the time required by other formal verification techniques."

RuleBase Parallel Edition offers support for the new PSL/Sugar standard property specification language. IBM RuleBase technology has been a cornerstone of the formal verification field since the early 1990s, and was among the first industrial formal verification solutions made available to engineers.

Over the last decade, RuleBase has been leveraged to verify ASICs and microprocessors developed by IBM and partners. The new RuleBase Parallel Edition platform takes advantage of the traditional strengths of IBM's technology, while embodying the results of IBM's newest research in the area of formal verification.

Using IBM's new static analysis methods, RuleBase Parallel Edition can verify a logic design against a set of PSL/Sugar assertions that represent the desired behavior of the design. To this end, RuleBase Parallel Edition employs two complementary schemes of parallel formal verification. The first scheme, 'fine-grained parallel FV' includes algorithms for the decomposition of a large verification task into smaller, tractable subtasks. These subtasks are solved in parallel by coordinated verification threads and are then conjoined to produce the solution for the original task. The second scheme, 'coarse-grained parallel FV' uses a sophisticated engine dispatcher, capable of distributing multiple verification tasks across a set of collaborating verification engines. To maximize verification performance, RuleBase Parallel Edition implements parallel formal verification on top of a large server farm via job-brokering software such as Load Sharing Facility (LSF) or Condor. In addition, RuleBase Parallel Edition provides a single, central point for controlling all verification tasks, thus optimally exploiting the computing power available in the underlying (possibly heterogeneous) network of workstations.

Parallel formal verification supports exhaustive state-space search and partial ("semiformal") search alongside traditional simulation of the design. Using a combination of these verification modalities, RuleBase Parallel Edition achieves a very high level of coverage, which can rapidly detect evasive design flaws that would have been very difficult to find using other verification methods.

"RuleBase Parallel Edition is the next-generation solution for making assertion-based verification a productive and extensive verification solution for the engineering community," Dr. Wolfsthal added. "By marrying massively parallel computing with formal verification, we have addressed two major problems: the size of the design it can verify and the time needed to verify that design. With RuleBase Parallel Edition, we have enabled the engagement of large simulation farms to achieve better, faster and more cost-effective formal verification."

RuleBase Parallel Edition runs on AIX, Solaris, and Linux and supports the standard property specification PSL/Sugar. IBM offers a demand-based licensing scheme to help users affordably leverage the unique capabilities enabled by the new tool.

Visit the RuleBase Parallel Edition Homepage at [http://www.haifa.il.ibm.com/projects/verification/RB\\_Homepage/index.html](http://www.haifa.il.ibm.com/projects/verification/RB_Homepage/index.html)

Reports on the successful application of IBM's functional formal verification solutions by IBM engineers and customers can be found at [http://www.haifa.il.ibm.com/projects/verification/Formal\\_Methods-Home/index.html](http://www.haifa.il.ibm.com/projects/verification/Formal_Methods-Home/index.html).


Example follows.

“We applied FFV to some extent on approximately 40 design components throughout the processor and found more than 200 design flaws at various stages and of varying complexity. At least one bug was found by almost every application of FFV. In most cases, FFV began significantly later than verification. **It is estimated that 15% of these bugs were of extreme complexity and would have been difficult for traditional verification.** In some cases, a late bug found in verification or in the laboratory was recreated and its correction verified efficiently with FFV.”

“FFV benefits on POWER4 included finding many complex bugs early, enhancing the block-level specification, ensuring that a block was ready for the next level of simulation, and reproducing traditional simulation bugs and laboratory bugs.”

Functional verification of the POWER4 microprocessor and POWER4 multiprocessor systems -  
Report by IBM engineers

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<p><b>IBM POWER4 System</b></p> <p>Vol. 46, No. 1, 2002</p> <p>Order No. G322- 0230</p>	<p>This issue contains five papers on the design of the IBM POWER4 Microprocessor and its use in the IBM eServer p690 "Regatta" system. Included are papers on the microarchitecture, circuit and physical design, fault-tolerant design, and functional verification of POWER4, and a paper describing the management and information-handling infrastructure for this large-scale multi-site development project. Also in the issue is a paper on pseudorandom-number generation using the fused multiply-add capabilities of IBM RISC-based processors.</p> <p><a href="#">click to enlarge →</a></p>	
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