



IBM Haifa Leadership Seminar - Agenda

Compiler and Architecture Seminar 2005

December 12, 2005

<http://www.haifa.il.ibm.com/Workshops/compiler2005/index.html>

Program

<p>9:15 Arrival</p> <p>9:30 Welcome, Oded Cohn, Director, IBM Haifa Labs</p> <p>9:45 Machine Learning Based Adaptive Optimizations, Mike O' Boyle, University of Edinburgh, UK</p> <p>10:15 Designing a Language and a Representation for Semi-automatic Program Transformation and Program Generation, Albert Cohen, INRIA, France</p> <p>10:45 Multi-platform Auto-vectorization, Dorit Naishlos, IBM HRL and Richard Henderson, RedHat</p> <p>11:15 Coffee Break</p> <p>11:35 Trace Cache Sampling Filter, Michael Behar, Technion; Avi Mendelson, Intel; Avinoam Kolodny, Technion</p> <p>12:05 Performance, Power Efficiency, and Scalability of Asymmetric Cluster Chip Multiprocessors, Tomer Y. Morad, Technion; Uri C. Weiser, Intel; Avinoam Kolodny, Technion; Mateo Valero, UPC, Spain; Eduard Ayguade, UPC, Spain</p>	<p>12:35 The Molen Compiler Backend for Reconfigurable Architectures, Elena Moscu, Koen Bertels, Stamatis Vassiliadis, TU Delft, The Netherlands</p> <p>13:05 Lunch</p> <p>14:00 Yonah - the First Intel CMP Architecture for Mobility, Ronny Ronen, Intel</p> <p>14:45 Compilation for the Cell processor, Kevin O'Brien, IBM Watson Research</p> <p>15:30 Break</p> <p>15:45 Automatic Parallelization with Hybrid Analysis, Lawrence Rauchwerger, Texas A&M University</p> <p>16:15 Experiences with Media-processing and Multi-processing, Henk Schepers, Philips</p> <p>16:45 Towards a Source Level Compiler: Source Level Modulo Scheduling, Yosi Ben-Asher and Danny Meisler, Haifa University</p> <p>17:15 Concluding Remarks</p>
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